

Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (withdrawn): A memory system comprising:
a plurality of storage cells that each store a data value; and
a memory control system that identifies particular ones of said storage cells as targets of read and write commands;
wherein data values written to ones of said plurality of storage cells identified by said memory control system identify tasks to be performed later;
wherein said memory control system determines an order of performing said tasks by controlling an order of reading data values from said plurality of storage cells;
wherein said memory control system reads out said data values so that a selected task is performed n times if and only if all other ones of said tasks have been performed n-1 times; and
wherein said memory control system allocates only one storage cell per task even if tasks are performed repeatedly.

Claim 2 (withdrawn): The memory system of claim 1 wherein said memory control system overwrites an oldest previously stored data value with a new data value.

Claim 3 (withdrawn): The memory system of claim 1 wherein said memory control system comprises:
a write pointer that identifies a next storage cell to be written to; and
a plurality of read pointers identifying a next storage cell to be read from, each of said plurality of read pointers associated with one of a plurality of priority levels.

Claim 4 (withdrawn): The memory system of claim 3 wherein said memory control system further comprises:
a plurality of registers, each of said registers identifying a number of storage cells implementing a particular list associated with one of said plurality of priority levels; .

Claim 5 (withdrawn): The memory system of claim 4 wherein one of said plurality of registers associated with a highest priority lists increments after each write operation.

Claim 6 (withdrawn): The memory system of claim 5 wherein said memory control system selects a particular storage cell for reading based on a value of a particular read pointer associated with a particular priority level.

Claim 7 (withdrawn): The memory system of claim 6 wherein said memory control system changes said current priority level to a next lower priority level when said register associated with said current priority level is zero and said register associated with said next lower priority level has a value greater than zero.

Claim 8 (withdrawn): The memory system of claim 6 wherein a register associated with a priority level one lower than a current priority level is decremented after a write operation that overwrites a value that has been read out using said read pointer associated with said current priority level.

Claim 9 (withdrawn): The memory system of claim 8 wherein said register associated with said priority level one lower than said current priority level decrements below zero.

Claim 10 (withdrawn): The memory system of claim 3 wherein said plurality of storage cells are each identified by a location in a circular address space and said write pointer and said read pointers store addresses in said address space.

Claim 11 (withdrawn): The memory system of claim 1 wherein said tasks comprise retransmissions of data in a communication system.

Claim 12 (withdrawn): The memory system of claim 1 wherein said tasks comprise requests for retransmission of data in a communication system.

Claim 13 (withdrawn): A memory system comprising:
a plurality of storage cells that each store a data value; and
a memory control system that identifies particular ones of said storage cells as targets of read and write commands;
wherein said memory control system determines an order of reading data values from said plurality of storage cells;
wherein said memory control system reads out said data values so that a data value is read out n times if and only if all other ones of said data values have been read out $n-1$ times; and
wherein said memory control system allocates only one storage cell per data value.

Claim 14 (previously presented): A method for operating a memory device including a plurality of storage cells:
dynamically partitioning said memory device into a plurality of priority lists;
directing new data to be stored in said memory device to storage cells belonging to a highest priority list of said plurality of priority lists;
reading data from said memory device only from a highest priority non-empty priority list; and
transferring said data read from said memory device from said highest priority non-empty priority list to a next lower priority list after reading without movement between storage cells;
and
wherein after reading said data and transferring said data, said data is maintained on said next lower priority list within said memory device.

Claim 15 (currently amended): The method of claim 14 wherein dynamically partitioning comprises:
providing a write pointer and a plurality of read pointers each of said read pointers corresponding to one of a plurality of priority levels corresponding to said plurality of priority lists.

Claim 16 (original): The method of claim 15 wherein directing comprises:
writing data to a location in said memory device determined by said write pointer and
thereafter incrementing said write pointer.

Claim 17 (original): The method of claim 15 wherein reading comprises:
reading data from a location in said memory device determined by one of said plurality of
read pointers corresponding to said highest priority non-empty priority list.

Claim 18 (original): The method of claim 17 wherein dynamically partitioning further
comprises:
providing for each of said priority lists a count register indicating an allocated number of
storage cells.

Claim 19 (currently amended): The method of claim 18 wherein transferring comprises:
incrementing said read pointer corresponding to said highest priority non-empty priority
list;
decrementing one of said count registers corresponding to said highest priority non-empty
priority list; and
incrementing one of said count registers corresponding to a next highest priority priority
list.

Claim 20 (previously presented): The method of claim 14 wherein said count register
corresponding to said next highest priority priority list is incremented only after a delay.

Claim 21 (previously presented): Apparatus for operating a memory device including a
plurality of storage cells:
means for dynamically partitioning said memory device into a plurality of priority lists;
means for directing new data to be stored in said memory device to storage cells
belonging to a highest priority list of said plurality of priority lists;

means for reading data from said memory device only from a highest priority non-empty priority list; and

means for transferring said data read from said memory device from said highest priority non-empty priority list to a next lower priority list after reading without movement between storage cells; and

wherein after reading said data and transferring said data, said data is maintained on said next lower priority list within said memory device.

Claim 22 (currently amended): The apparatus of claim 21 wherein said means for dynamically partitioning comprises:

means for providing a write pointer and a plurality of read pointers each of said read pointers corresponding to one of a plurality of priority levels corresponding to said plurality of priority lists.

Claim 23 (previously presented): The apparatus of claim 22 wherein means for directing comprises:

means for writing data to a location in said memory device determined by said write pointer and thereafter incrementing said write pointer.

Claim 24 (previously presented): The apparatus of claim 22 wherein said means for reading comprises:

means for reading data from a location in said memory device determined by one of said plurality of read pointers corresponding to said highest priority non-empty priority list.

Claim 25 (previously presented): The apparatus of claim 24 wherein said means for dynamically partitioning further comprises:

means for providing for each of said priority lists a count register indicating an allocated number of storage cells.

Claim 26 (previously presented): The apparatus of claim 25 wherein said means for transferring comprises:

means for incrementing said read pointer corresponding to said highest priority non-empty priority list;

means for decrementing one of said count registers corresponding to said highest priority non-empty priority list; and

means for incrementing one of said count registers corresponding to a next highest priority priority list.

Claim 27 (previously presented): The apparatus of claim 26 wherein said count register corresponding to said next highest priority priority list is incremented only after a delay.

Claim 28 (previously presented): The method of claim 14 wherein said data read from said memory device represents a retransmission task.

Claim 29 (currently amended): The apparatus of claim ~~29~~ 21 wherein said data read from said memory device represents a retransmission task.

Claim 30 (previously presented): Apparatus for storing data, said apparatus comprising:
a memory device dynamically partitioned into a plurality of priority lists, wherein new data to be stored in said memory device is directed to storage cells belonging to a highest priority list of said plurality of priority lists; and

a memory control engine that reads data from said memory device only from a highest priority non-empty priority list, transfers said data read from said memory device from said highest priority non-empty priority list to a next lower priority list after reading without movement between storage cells; and

wherein after reading said data and transferring said data, said data is maintained on said next lower priority list.

Claim 31 (currently amended): The apparatus of claim 30 wherein said memory control engine comprises:

a write pointer and a plurality of read pointers each of said read pointers corresponding to one of a plurality of priority levels corresponding to said plurality of priority lists.

Claim 32 (previously presented): The apparatus of claim 30 wherein said memory control engine further comprises:

a count register for each of said priority lists indicating an allocated number of storage cells.

Claim 33 (previously presented): The apparatus of claim 32 wherein said count register corresponding to said next highest priority list is incremented only after a delay.